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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: 40296-0007

Applicant(s):	Seung Cheol Bae	Confirmation No.:	8519
Appl. No.:	10/608,292	Examiner:	Minh T Nguyen
Filing Date:	06/30/2003	Art Unit:	2816
Title:	SETUP/HOLD TIME CONTROL DEVICE		

Amendment & Reply

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant herein responds to the Office Action mailed May 5, 2004, for the above-captioned application.

Please reconsider the Application as follows.

Amendments

1. (Currently Amended) A device for controlling a setup/hold ~~setup/hole~~ time of an input signal ~~control apparatus~~, comprising:

a driver for outputting a global bus line control signal by amplifying ~~driving~~ an output signal ~~of an~~ from an input buffer;

a signal delay unit for delaying the global bus line control signal selectively connected to the driver;

a decoding unit for outputting a test mode delay signal by decoding a test control signal for determining to control setup/hold time corresponding to the global bus line control signal, a test mode entry signal, and a test mode exit signal ~~end signal~~; and

a delay control unit for controlling the ~~setup/holde~~ setup/hold time of the global bus line control signal by selectively connecting the signal delay unit to the driver according to a state of the test mode delay signal.

2. (Currently Amended) The device for controlling a setup/hold time of an input signal ~~control device~~ according to claim 1, further comprising a first latch for latching ~~and outputting~~ the global bus line control signal in synchronous to ~~synchronization with~~ a clock signal.

3. (Currently Amended) The device for controlling a setup/hold time of an input signal ~~control device~~ according to claim 1, wherein the driver comprises an inverter chain including an even number of inverters connected in series for ~~non-inverting and~~ delaying and logically non-reversing the output ~~an output~~ signal from the ~~of the~~ input buffer ~~connected in series~~.

4. (Currently Amended) The device for controlling a setup/hold time ~~control device~~ of an input signal according to claim 1, wherein the signal delay unit comprises:

a first capacitor unit connected selectively to a first node of the driver controlled by the delay control unit; and

a second capacitor unit connected selectively to a second node of the driver controlled by the delay control unit.

5. (Currently Amended) The device for controlling a setup/hold time of an input signal ~~control device~~ according to claim 4, wherein the first capacitor unit and the second capacitor unit are MOS capacitors.

6. (Currently Amended) The device for controlling a setup/hold time of an input signal ~~control device~~ according to claim 4, wherein the delay control unit comprises:

a first delay control unit for delaying the setup/hold time of the global bus line control signal by selectively connecting the first capacitor unit to the first node according to ~~a state of~~ a first state of the test mode delay signal; and

a second delay control unit for advancing the setup/hold time of the global bus line control signal by selectively connecting the second capacitor unit to the second node according to ~~a state of~~ a second state of the test mode ~~test moe~~ delay signal.

7. (Currently Amended) The device for controlling a setup/hold time of an input signal ~~control device~~ according to claim 6, wherein the first delay control unit comprises a first transmission gate and a second transmission gate for receiving the ~~first~~ test mode delay signal through a NMOS gate, and receiving an inversion of the ~~first~~ test mode delay signal ~~inverted~~ through a PMOS gate to selectively connect the first MOS capacitor unit to the first node.

8. (Currently Amended) The device for controlling a setup/hold time ~~control device~~ of an input signal according to claim 6, wherein the second delay control unit comprises a third transmission gate and a fourth transmission gate for receiving the ~~second~~ test mode delay signal through a PMOS gate, and receiving an inversion of the ~~second~~ test mode delay signal ~~inverted~~ through a NMOS gate to selectively connect the second capacitor unit to the second node.

9. (Currently Amended) The device for controlling a setup/hold time ~~control device~~ of an input signal according to claim 6, wherein the decoding unit connects the first capacitor

unit to the first node by ~~outputting~~ setting the ~~first~~ test mode delay signal ~~at a~~ high ~~level~~ when the test control signal is at a high level, and disconnects ~~intercepts connection between~~ the second capacitor unit and the second node by ~~outputting~~ setting the ~~second~~ test mode delay signal ~~at a~~ high ~~level~~ when the test control signal is at a low level.

10. (Currently Amended) The device for controlling a setup/hold time ~~control device~~ of an input signal according to claim 9, wherein the decoding unit comprises:

a logic unit for logically operating the test control signal and the test mode entry signal to output a first output signal and a second output signal;

a second latch for latching the ~~first~~ test mode delay signal according to the first output signal and the test mode exit signal ~~end signal~~; and

a third latch for latching the second test mode delay signal according to the second output signal and the test mode exit signal ~~end signal~~.

11. (Currently Amended) The device for controlling a setup/hold time of an input signal ~~control device~~ according to claim 10, wherein the logic unit comprises:

a first NAND gate for NANDing the test control signal and the test mode entry signal to output the first output signal; and

a second NAND gate for NANDing the test mode entry signal and ~~the inverted test mode entry~~ inverted of the test control signal to output the second output signal.

12. (Currently Amended) The device for controlling a setup/hold time ~~control device~~ of an input signal according to claim 10, wherein the second latch comprises a third ~~thrid~~ NAND gate and a fourth NAND gate that are cross-coupled to ~~for feeding back each output signal as an input signal~~ each other.

13. (Currently Amended) The device for controlling a setup/hold time ~~control device~~ of an input signal according to claim 10, wherein the third latch comprises a fifth NAND gate and a sixth NAND gate that are cross-coupled to ~~for feeding back each output signal as an input signal~~ each other.